Front end electronics for semiconductor detectors in HEP

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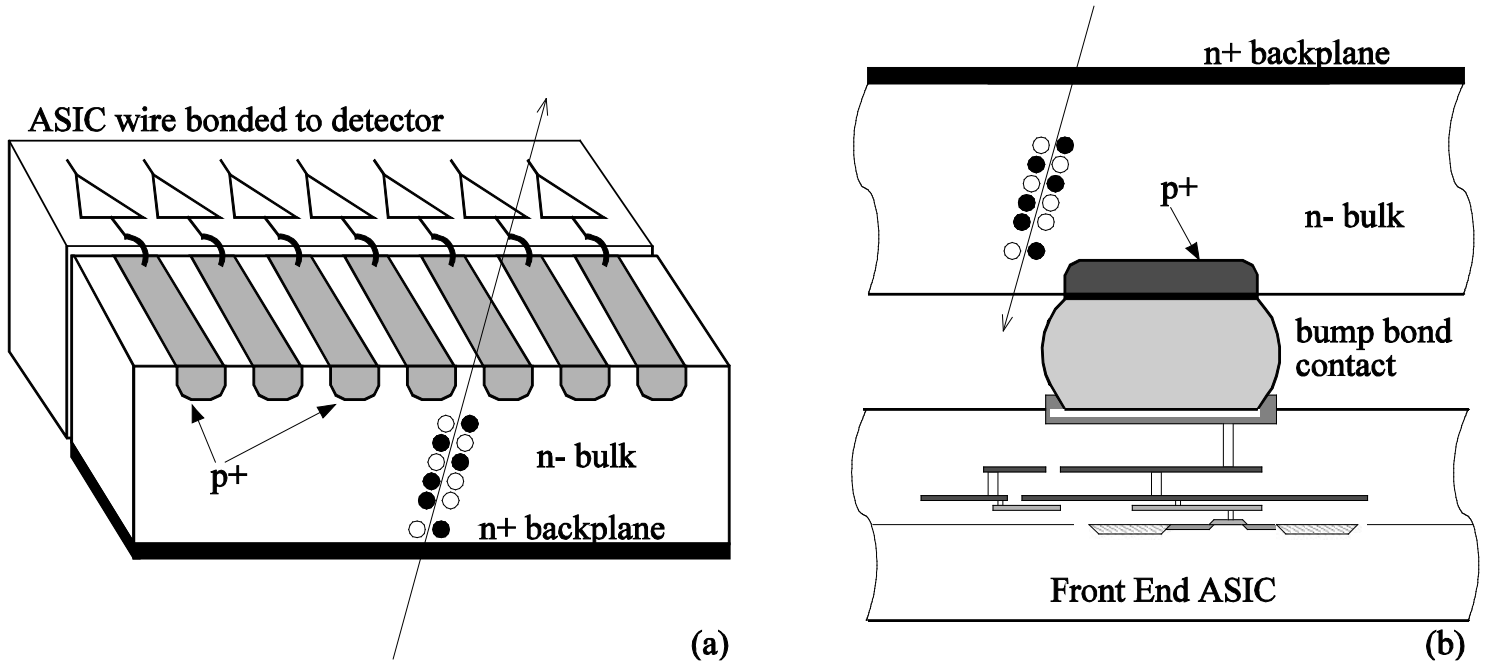
Outline

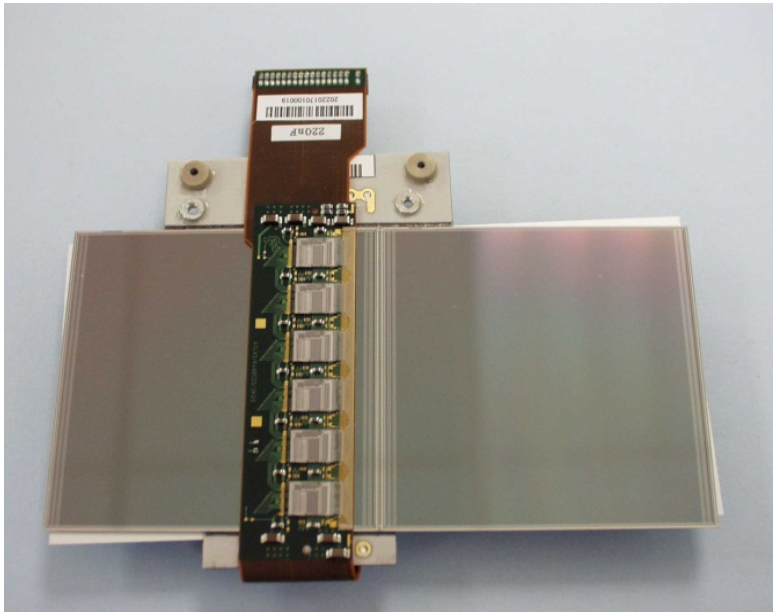
- Principles of semiconductor detectors
- Driving issues for designing of front end electronics:
  - charge collection efficiency and cross talk signals
  - noise and power
  - PSRR
- Consequences of technology scaling
- Basic configuration of feedbacks and architectures of the input stages
- Some examples of front end stages

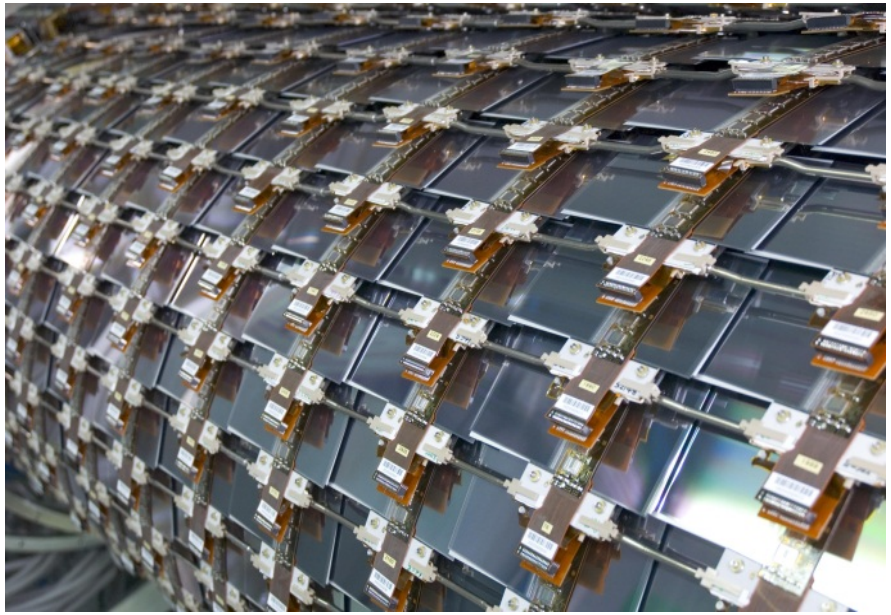
Principles of semiconductor detectors for tracking applications



- p^+ n junction reverse biased forms the detection zone
- Ionization along the track of the high-energy particle or photoelectric absorption of γ quant
- For 300µm Si detector the most probable signal is around 3.5 fC (MIP)
- Electric field proportional to bias provides drifting of the created charge pairs – induced current is read out by the front-end electronics
- Spatial resolution provided by the segmentation of the detector

From single crystal to system





Double sided silicon strip detector module of ATLAS experiment at CERN/Geneva, (left). The module consists of four, 6.5 by 6.5 cm silicon detectors (two daisy-chained back to back) and it is equipped with 12 (6 on each side) 128 channel front end ASICs.

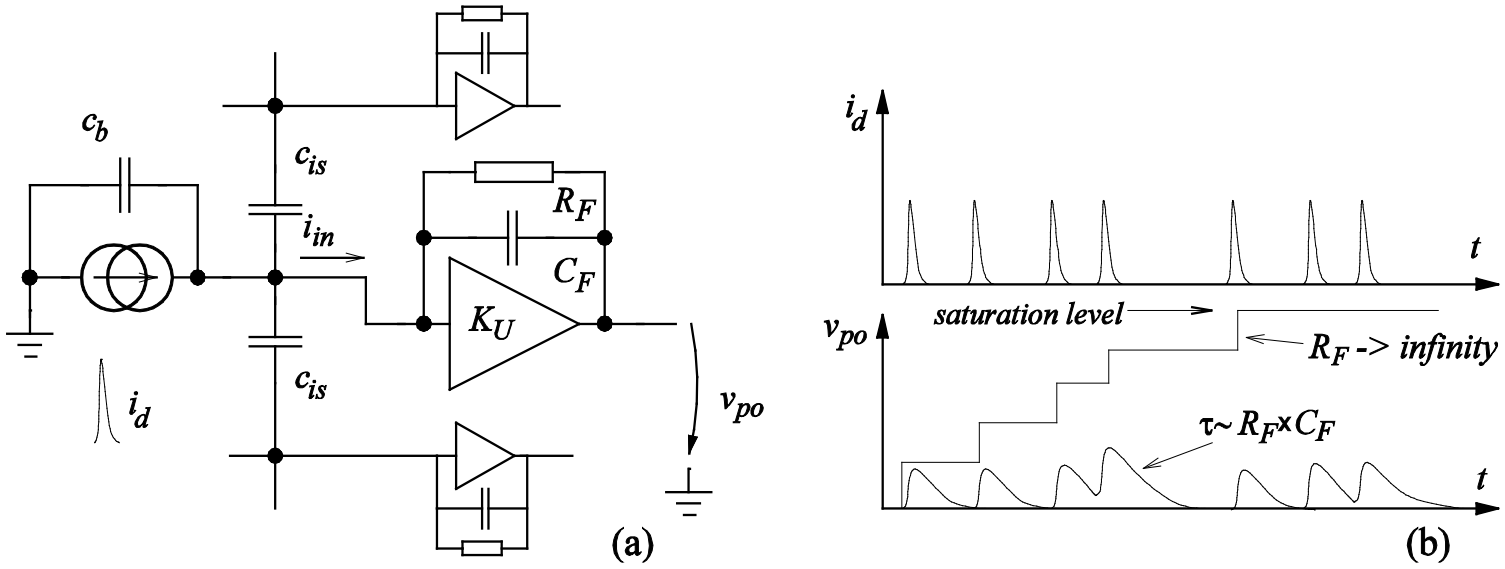
One barrel layer of the ATLAS SemiConductor Tracker, 4088 modules, 61m^2 (right).

Multichannel systems in confined space → power consumption one of the critical issue.

Another requirements: noise performance, response time, stability, PSRR, rad-hardness

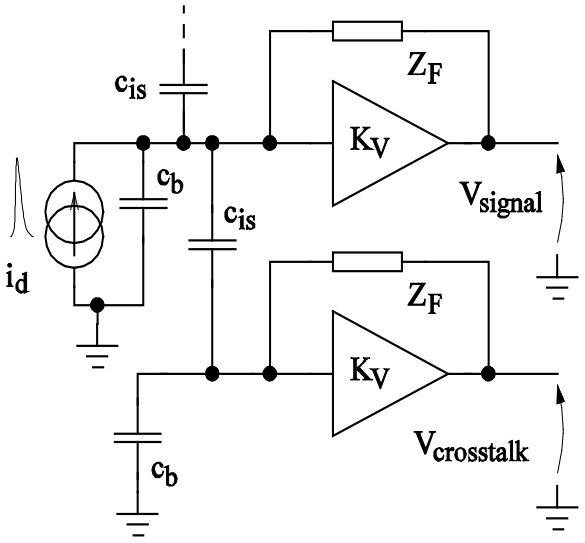
Signal reception and cross-talk

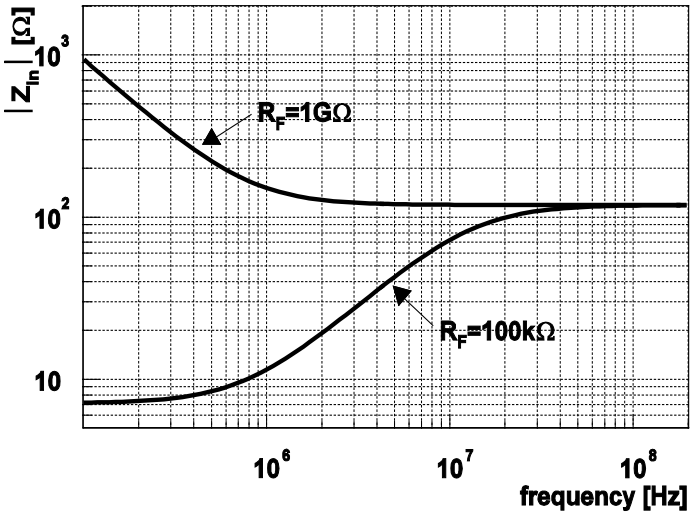
Reception of signals from silicon detector



- Detector represented by parasitic capacitance, signal represented by current pulse (Dirac-Delta)
- Charge sensitive preamplifier
  - Dirac-Delta current pulses integrated on feedback capacitance (smaller capacitance → higher signal gain)
  - Discharge provided by the feedback resistor (prevents saturation)
- Mode of the preamplifier is defined by feedback time constant $\tau_F = R_F C_F$ (transimpedance or charge amplifier)

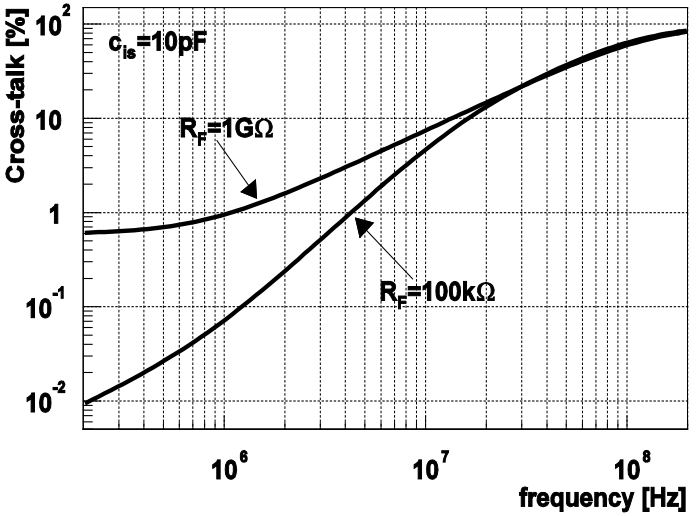
Input impedance and cross-talk signals





$$Z_{IN}(s) \approx \frac{Z_F(s)}{K_V(s)} \qquad K_V(s) = \frac{K_V}{1 + s \cdot \tau_{P0}}$$

$$Cross\ Talk\ (s) = \frac{Z_{IN}(s)}{Z_{IN}(s) + Z_{IS}(s)}$$



Input impedance and cross-talk for amplifier with 83dB gain and 1GHz Gain Bandwidth Product (GBP) working in charge and transimpedance configurations

Cross talk in time domain

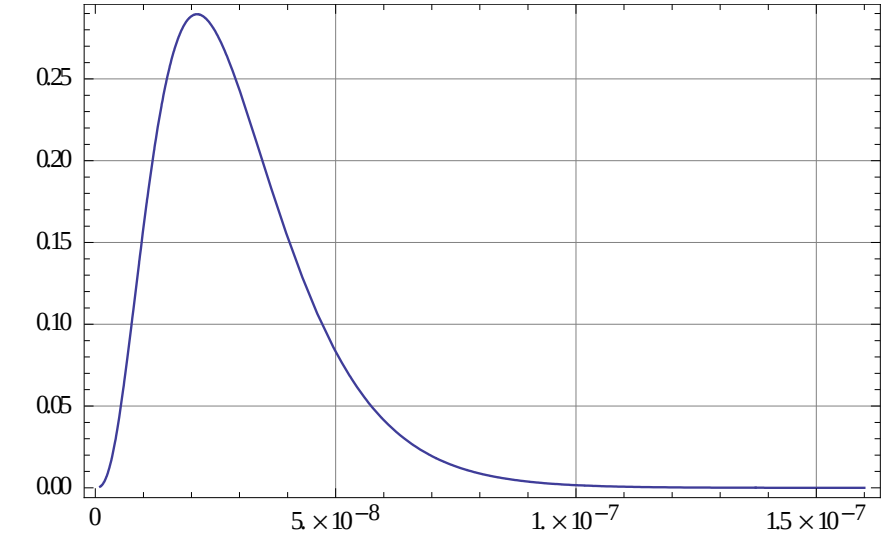
A naive approach to the crosstalk problem:

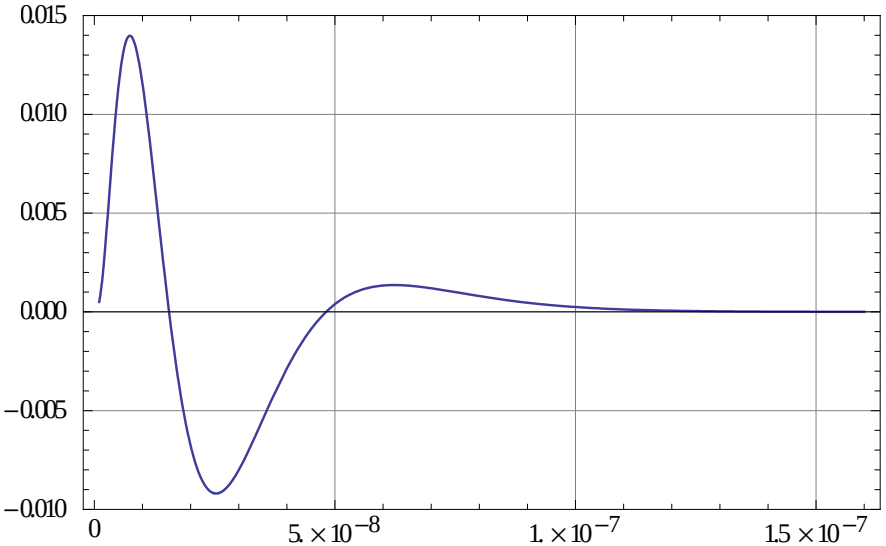
We loose 1% charge in the readout channel (e.g. due to the input impedance) so we can expect that the signal seen in one neighbor will be 0.5% → wrong!

Unfortunately, the amplitude of the cross talk w.r.t. signals readout from detector, because of different frequency spectra, can be much higher than the percentage of the lost charge

Analytical approach possible by use of Laplace transform.

Example of crosstalk calculation for transimpedance mode





Kv=83dB, τ_{p0} =200ns, GBP=1GHz *)

Detector; c_{is}=7pF, c_b=4pF (ATLAS SCT)

Response; Max=0.289 for t=21ns
(0.27 for 20ns without detector)

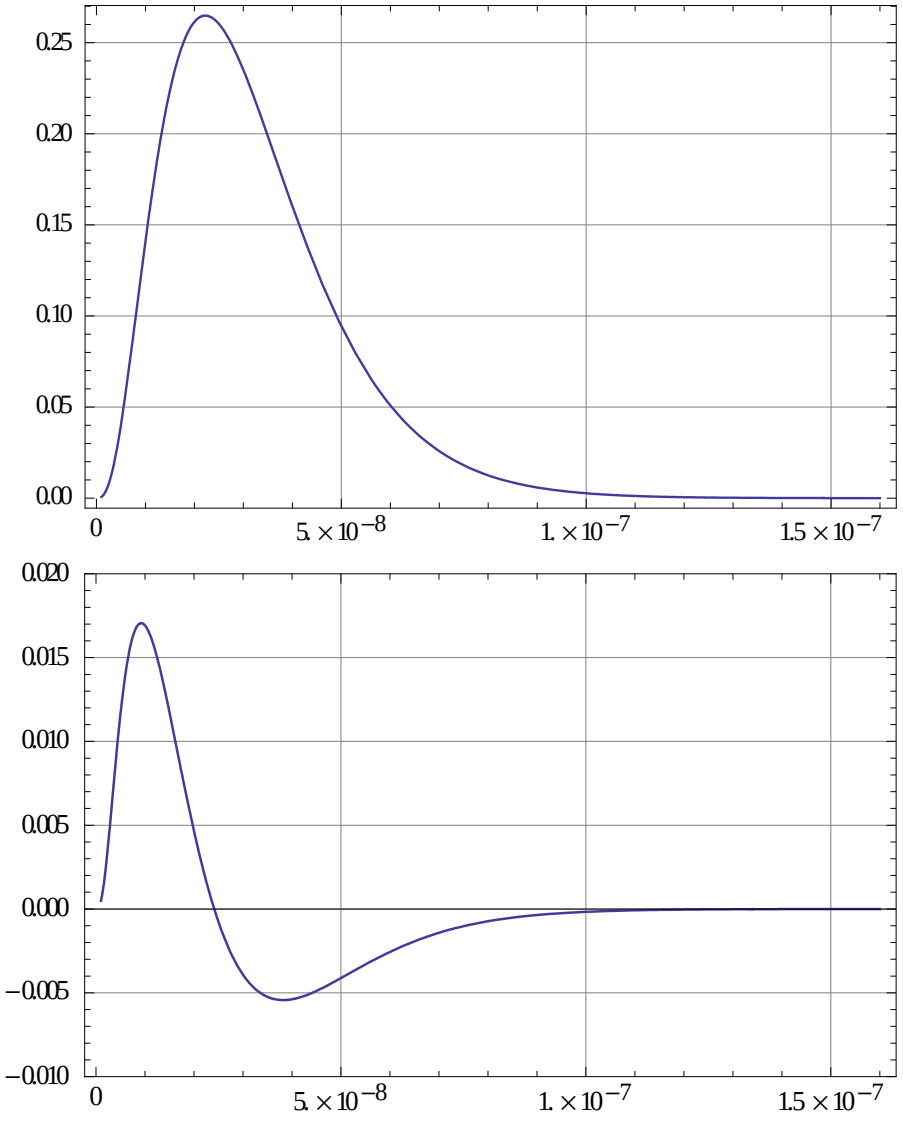
$$\int_0^\infty i_s(t)\,\partial t = 1$$

The overall charge readout by front end for transimpedance preamplifier is full!

Crosstalk; Max=0.0139 for t=7.4ns (5%)

Design presented in; J. Kaplon and W. Dabrowski, "Fast CMOS binary front end for silicon strip detectors at LHC Experiments," *IEEE Trans. Nucl. Sci.*, vol. 52, no. 6, pp. 2713–2720, Dec. 2005

Example of crosstalk calculation for charge preamp



Kv=83dB, τ_{p0} =200ns, GBP=1GHz *)

Detector; c_{is}=7pF, c_b=4pF (ATLAS SCT)

Response; Max=0.265 for t=22.2ns
(0.27 for 20ns without detector)

$$\int_0^\infty i_s(t)\,\partial t = 0.99$$

Lost of charge related to finite open loop gain of the preamplifier!

Crosstalk; Max=0.017 for t=9.2ns (~6.5%)

Preamplifier stage the same as in the last slide but working in charge mode (very high RF, CR-RC2 filter build with shaper only)

To minimize crosstalk:

- for SLHC strip detectors (few pF detector capacitances) the optimal open loop gain of the preamplifier should be around 70 to 80dB (in order to provide cross talk less than 5%)
- for pixel detectors ~50 dB open loop gain sufficient
- for peaking time around 20 ns as for SLHC the GBP should be above 1 GHz
- transimpedance amplifiers better than charge amplifiers (but the difference is moderate)

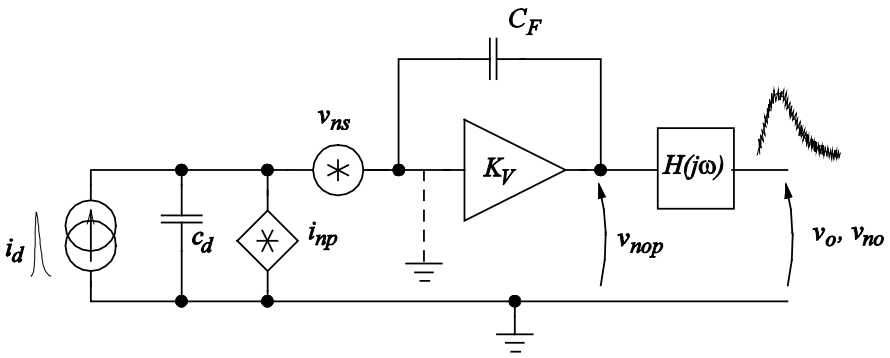
Minimizing noise and power

Noise/power optimisation

Low noise at minimum power:

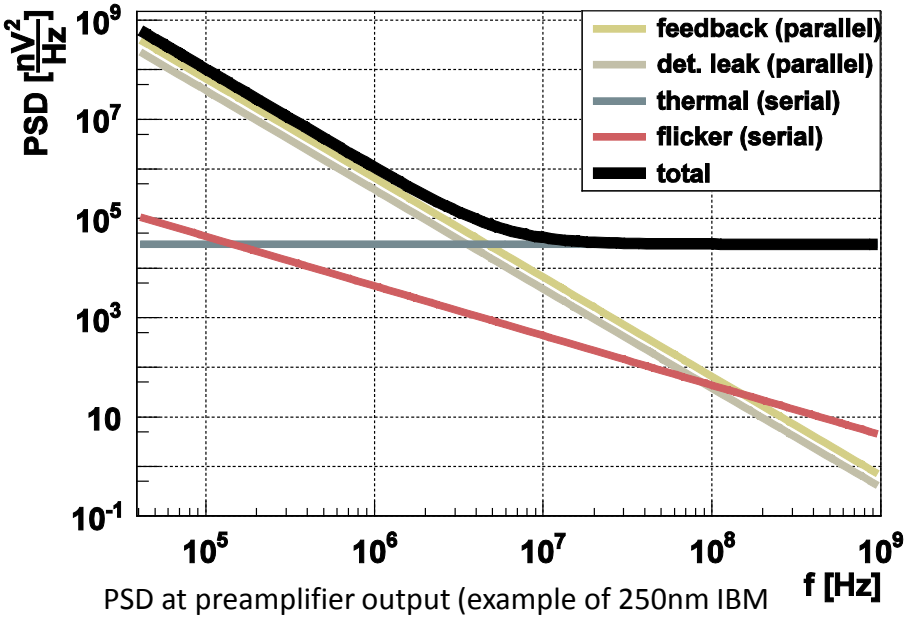
- limiting the serial noise contribution to the one, input transistor:
  - single ended architecture (compatible with the construction of the sensor)
  - high signal gain of the input stage (to limit contribution from following stages)
  - careful design of the active load (degeneration of current sources), proper bias for the regulated cascode
- optimization of the input transistor (type, dimensions)
- evaluation of the parallel noise sources (detector leakage, choice of the preamplifier feedback type)
- noise filtration

Principle of noise filtration for CSA



$$\frac{\overline{v_{nop}^2}}{\Delta f} = \frac{\overline{v_{ns}^2}}{\Delta f} \cdot \frac{c_d^2}{C_F^2} + \frac{\overline{i_{np}^2}}{\Delta f} \cdot \frac{1}{\omega^2 \cdot C_F^2}$$

$$\sigma_{nfo}^2 = \int_0^\infty \frac{\overline{v_{nop}^2}}{\Delta f} \cdot |H(j\omega)|^2 \quad \partial f$$

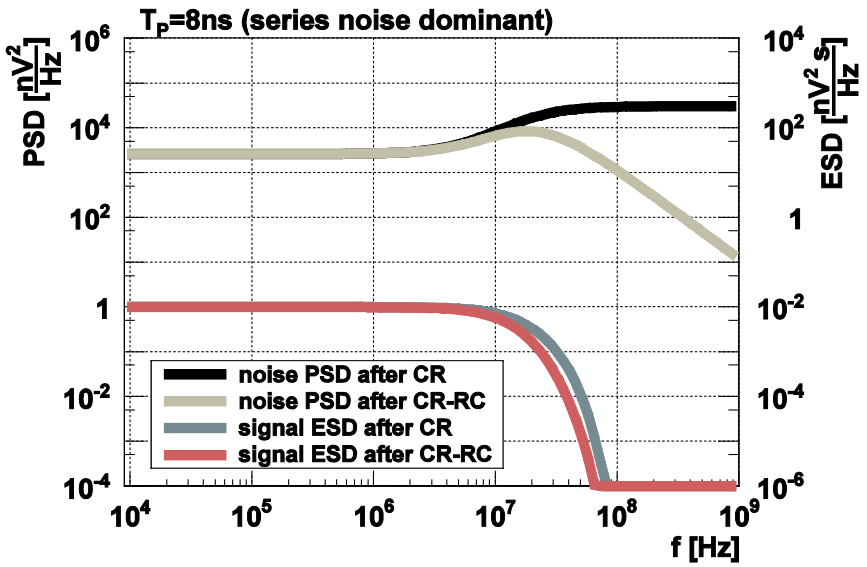


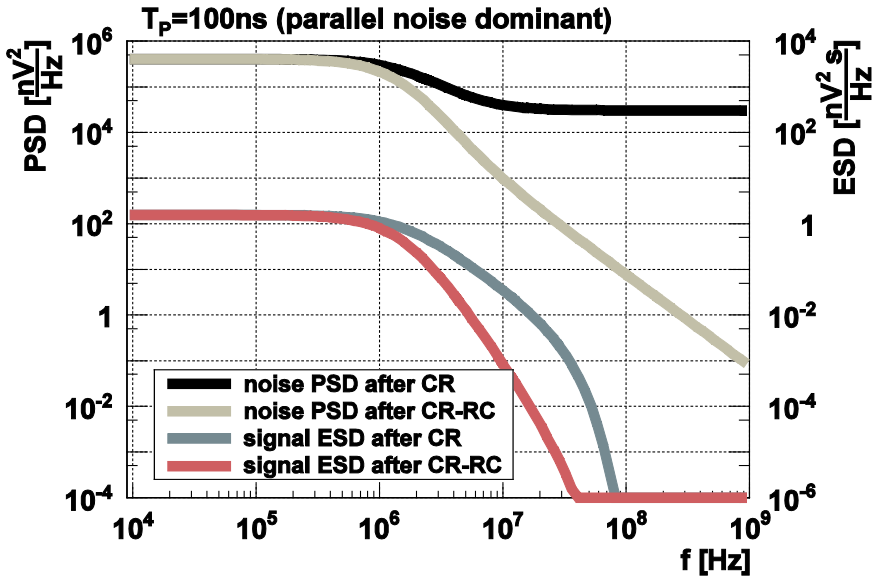
PSD at preamplifier output (example of 250nm IBM design optimized for short strips);

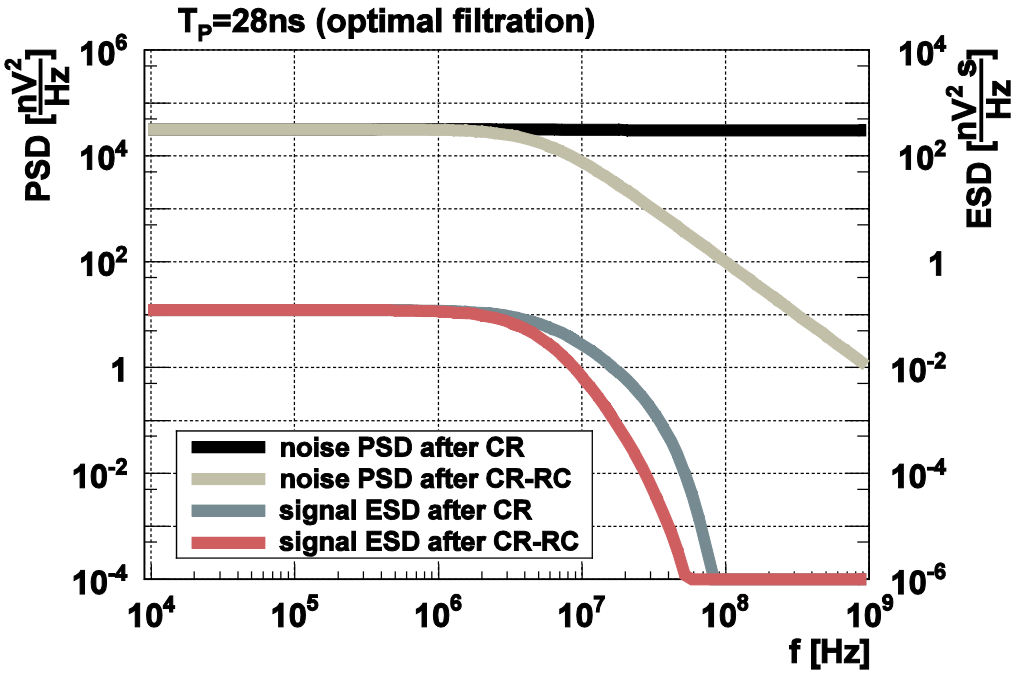
- C_d = 5 pF, C_F=80 fF
- Input transistor NMOS 320/0.5, Id=140uA (gm=4mS)
- Rfeed=100 kOhm
- Det. Leak=300 nA

To converge the integral, the filter should consist of "whitening" section for low frequencies (parallel noise contribution) and low pass section (bandwidth limitation for high frequency) → CR-RC filters

Noise and signal spectra's for CR-RC filters







- optimum time constant of CR-RC filter usually longer than requested by the timing condition of LHC experiments
- reduction of serial noise contribution (thermal noise of the MOS channel, shot noise of BJT) by increase of g_m of the input transistor

Noise optimisation of g_m <-> c_{gate} for input transistor (EKV transistor model)

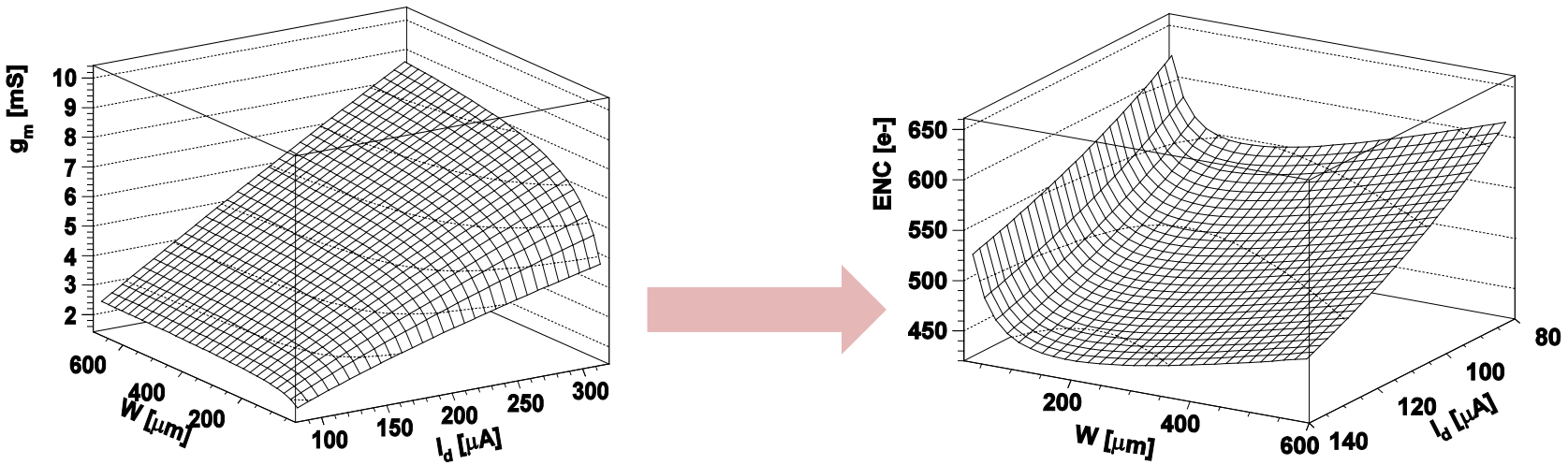
Transconductance:

$$g_m = G(I_f) \cdot \frac{I_D}{n \cdot U_T}$$

g_m in weak inversion

$$I_S = 2 \cdot n \cdot K_P \cdot \frac{W}{L} \cdot U_T^2 \qquad U_T = \frac{k \cdot T}{q} \qquad G(I_f) = \frac{1}{\sqrt{I_f + \frac{1}{2} \cdot \sqrt{I_f} + 1}}$$

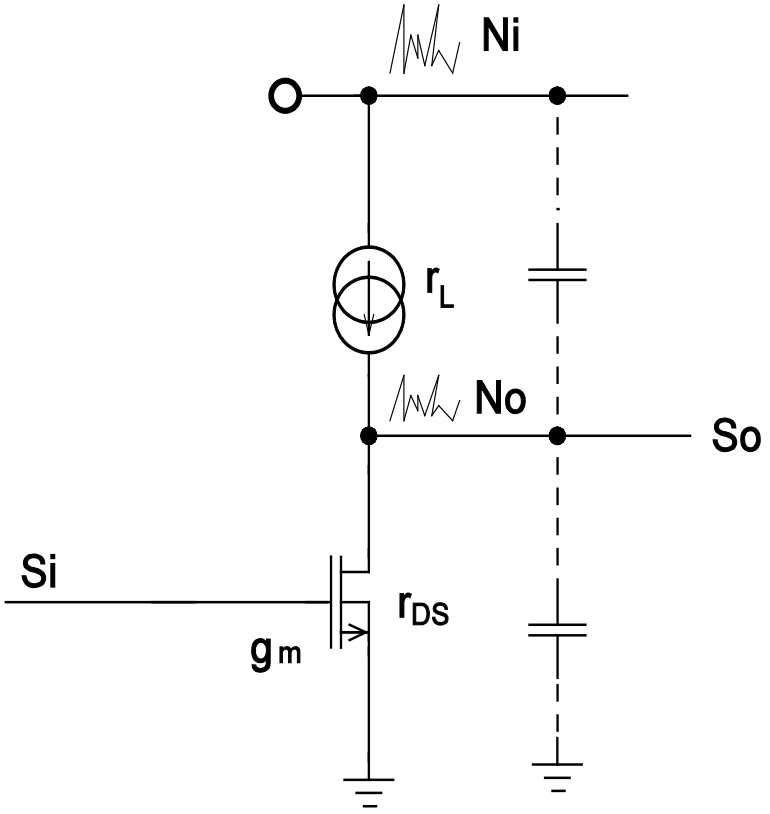
Optimization for IBM 130nm NMOS L=300nm and Cd=5pF



Usually optimisation leads to operating of the transistors in weak or moderate inversion regions.

PSRR in single ended stages

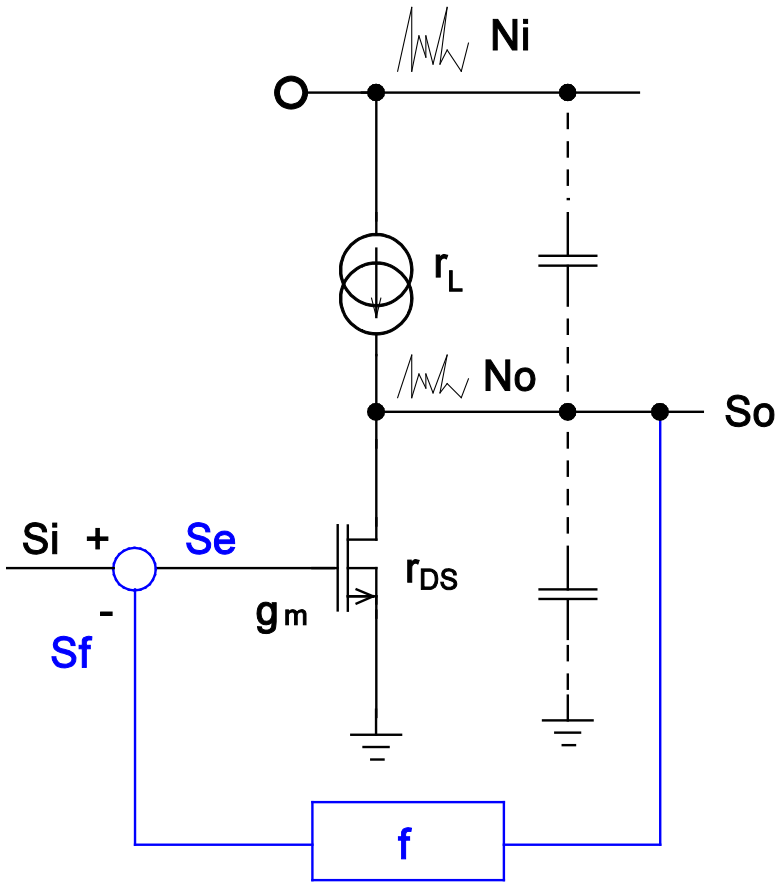
PSRR for single ended stage (1)



$$K_U = \frac{So}{Si} = g_m \cdot \left(r_L \parallel r_{DS}\right)$$

$$N_O = N_i \cdot \frac{Z_{DS}(s)}{Z_{DS}(s) + Z_L(s)}$$

PSRR for single ended stage (2)

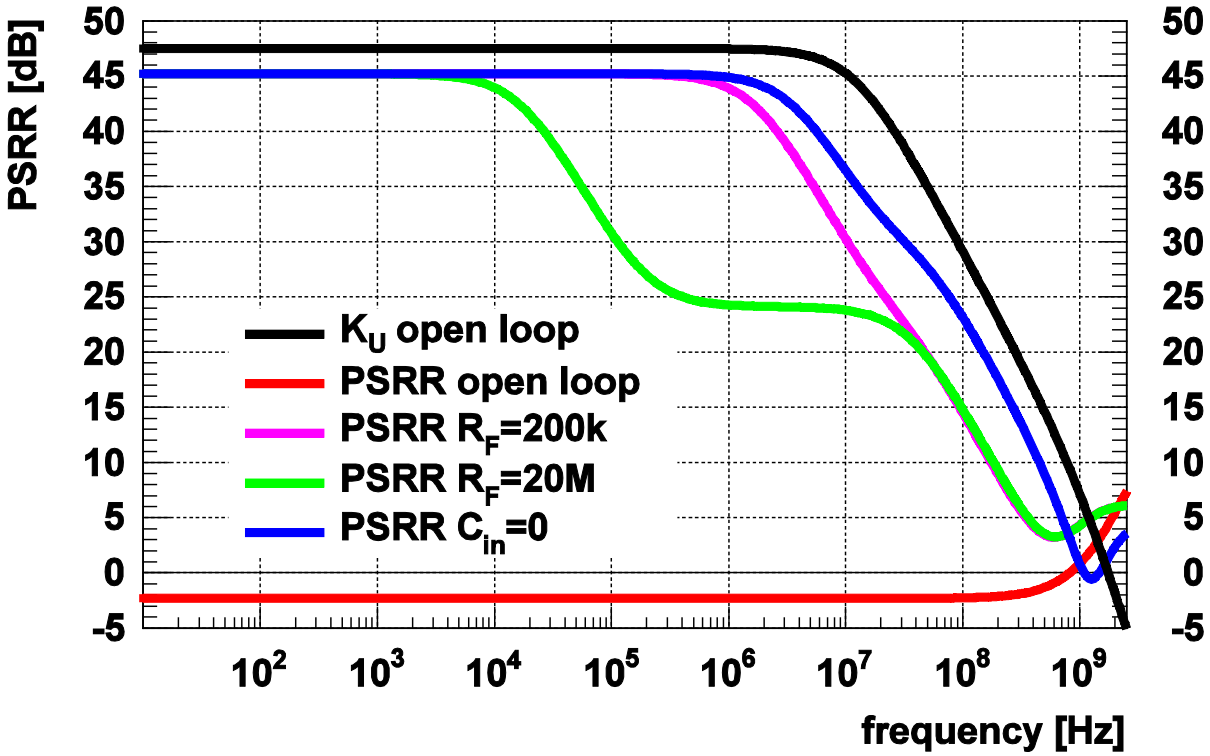


$$S_O = K_U \cdot S_e + N_O$$
$$S_f = f \cdot S_O$$
$$S_e = S_i - S_f$$

$$S_O = S_i \frac{K_U}{1 + K_U \cdot f} + N_O \frac{1}{1 + K_U \cdot f}$$

Driving K_U improves PSRR.
All single ended stages should be designed as feedback amplifiers with high open loop gain.

PSRR for single ended stage (3)



Open loop gain and PSRR characteristics of cascode preamplifier for a fast pixel front end implemented in 130nm CMOS.

Motivations to increase open loop gain (input stage)

- Lower input impedance of preamplifier;
  - better charge collection efficiency
  - lower cross talk
- Optimizing feedback impedance (i.e. signal gain of the preamplifier) versus input impedance → charge collection efficiency, crosstalk signals and noise contribution from following stages
- PSRR (all single ended stages)

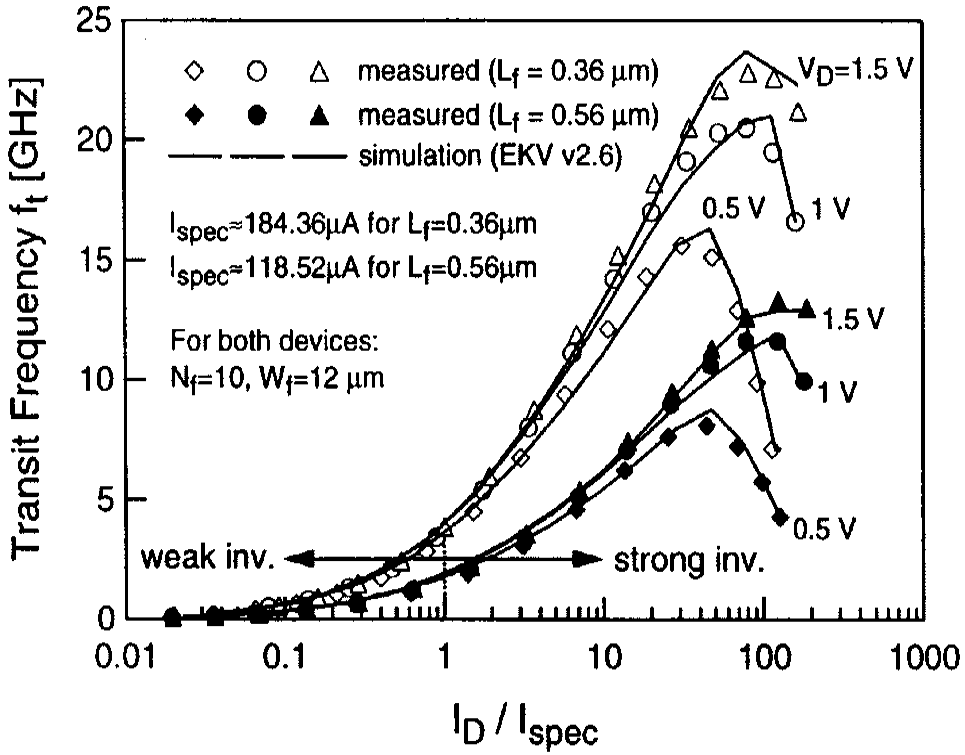
Consequences of technology scaling

IBM CMOS	250nm RF (IBM)	130nm RF (IBM)	65 nm LP (TSMC)
t_{OX}	5nm	2.2nm	2.6nm
K_p@Ispec NMOS	330 uA/V^2	720 uA/V^2	320 uA/V^2
Vdd	2.5V	1.2V (1.5V)	1.2V
g_m/g_{ds} moderate inv. (example for input transistor)	70 (l=500nm)	30 (l=300nm)	18 (l=140nm)
Peak ft	35 GHz	94 GHz	240 GHz

- Advantages:
  - higher f_t and transconductance (but not always → see TSMC example)
- Drawbacks:
  - Lower intrinsic gain and supply voltage
    - solution: cascode and regulated cascode architecture
    - preferable operating point: weak or moderate inversion (minimum Vdd_{SAT})

Weak inversion: some consequences

Inversion order versus the speed of CMOS circuit

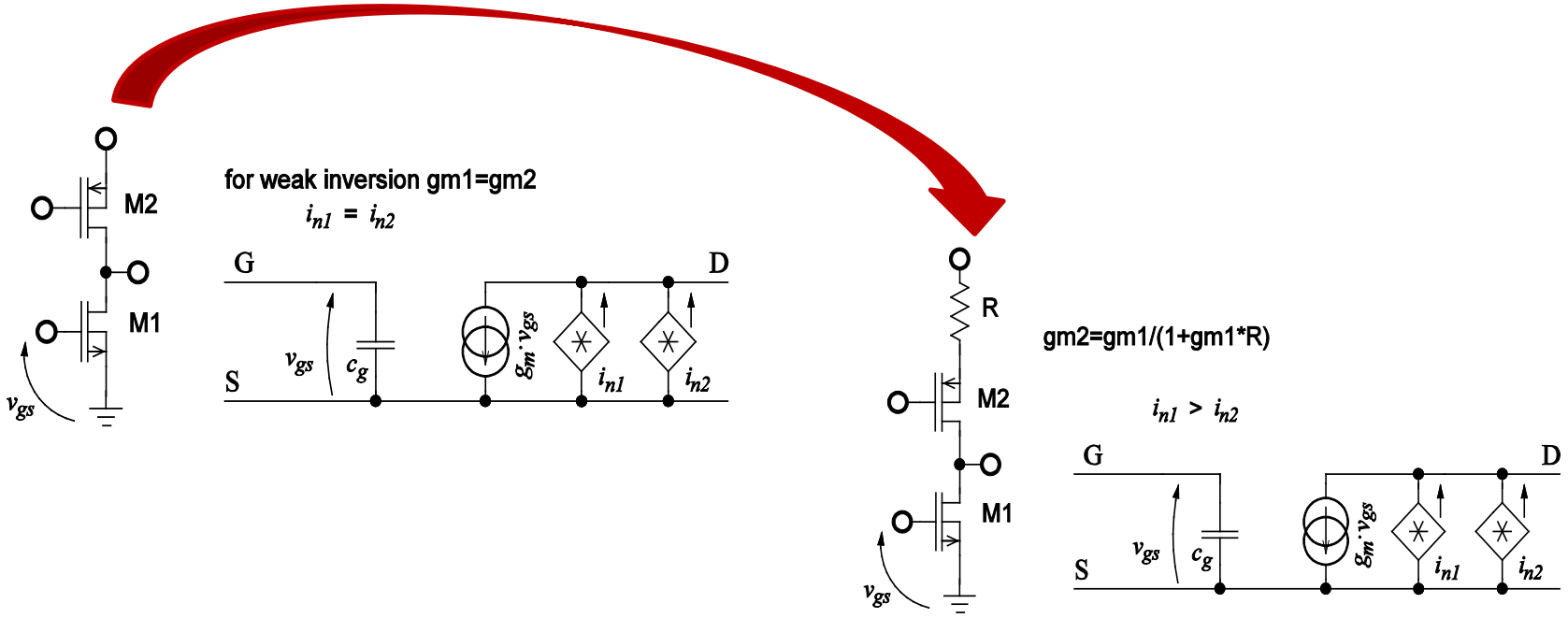


Transit frequency ft as a function of inversion order for 250nm CMOS technology *

For devices biased in weak inversion we never obtain highest possible speed of a given technology

* C.Enz, "MOS transistor modeling for RF IC design", *IEEE J.Solid-State Circ.,* vol. 35, no. 2, pp.186-201)

Noise of the active load



If all transistors are in weak inversion then the g_m is defined only by current → all g_m the same

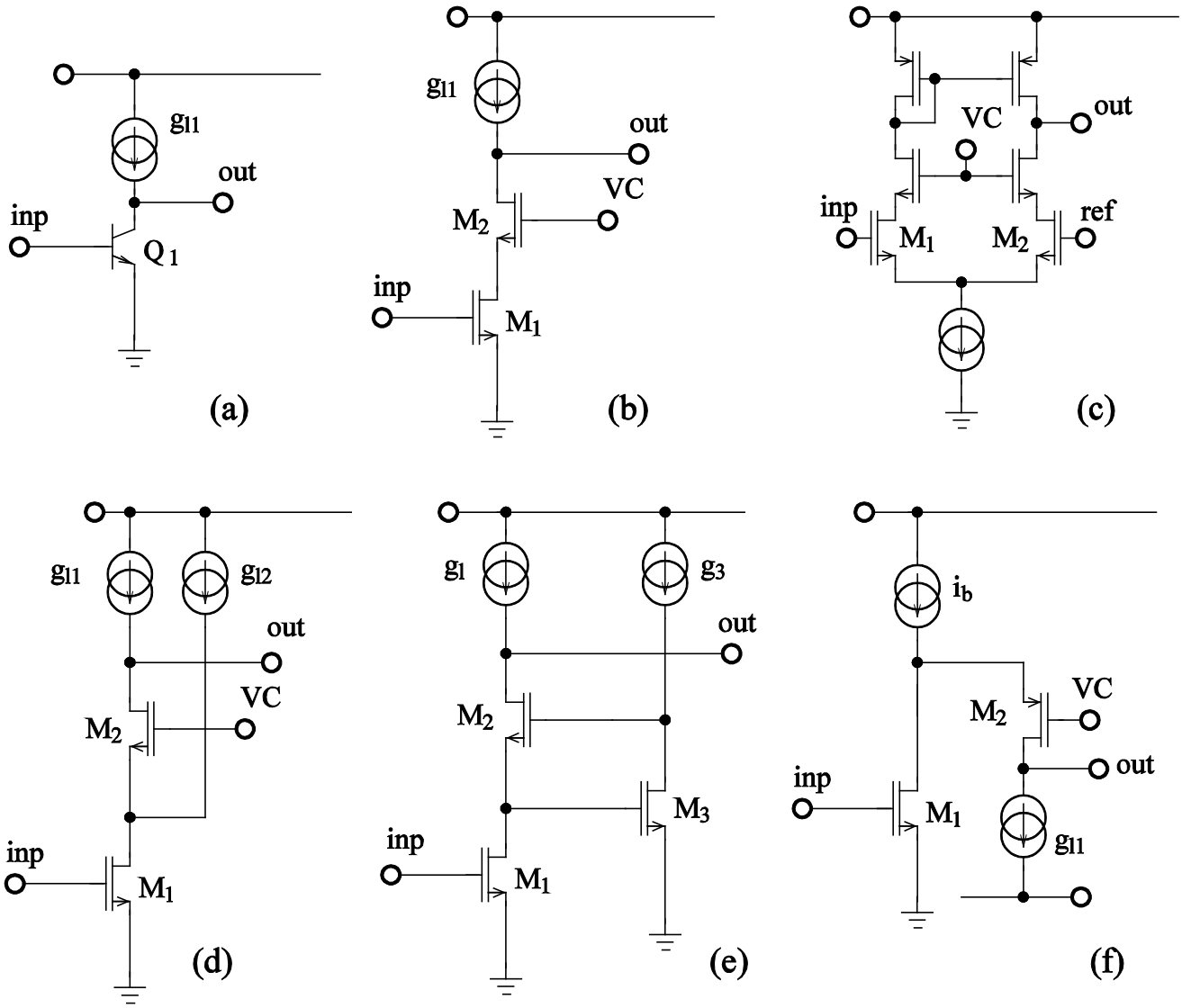
Increase of input series noise by ~40%!

Resistive degeneration of g_m works

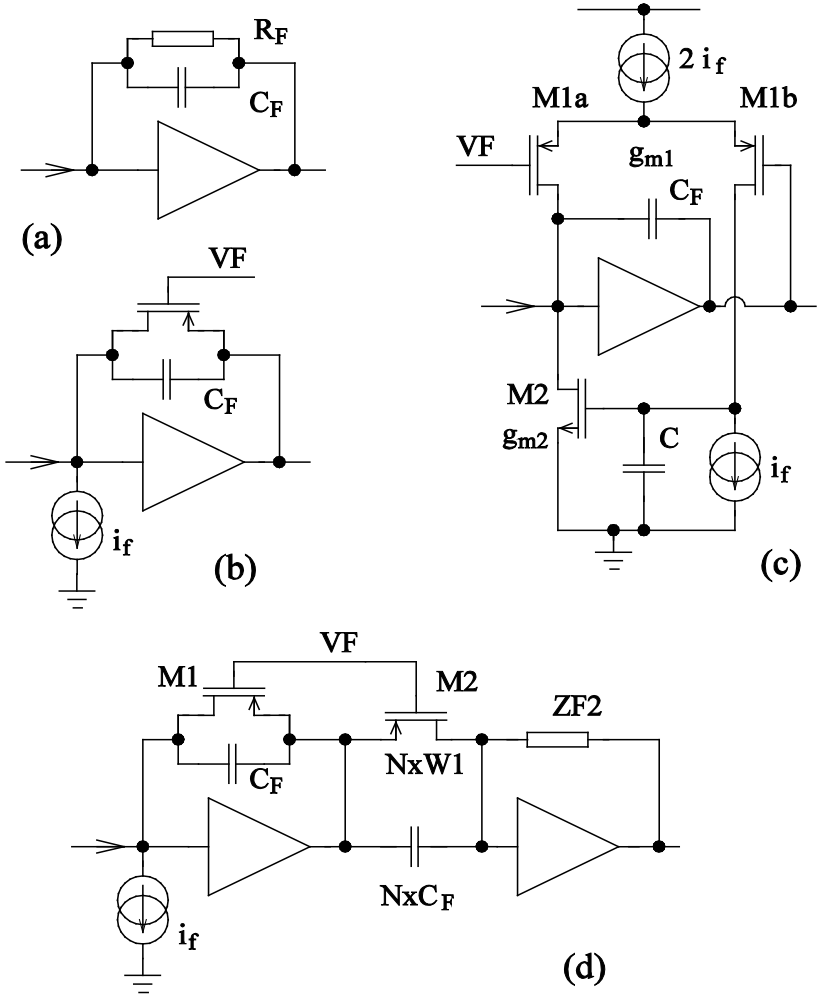
But we have to spend another ~100mV taken out from Vdd…

Examples of the front end amplifiers

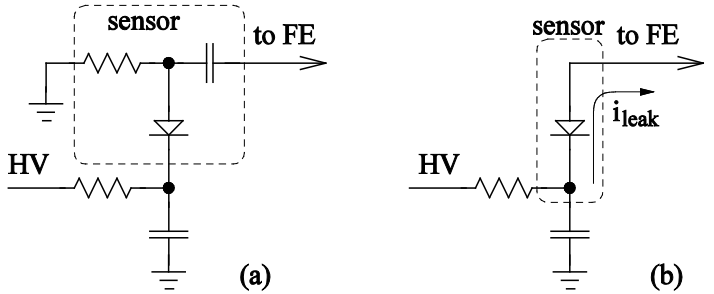
Basic architectures for the input stage



Basic configurations of feedback



Types of detector coupling: AC and DC



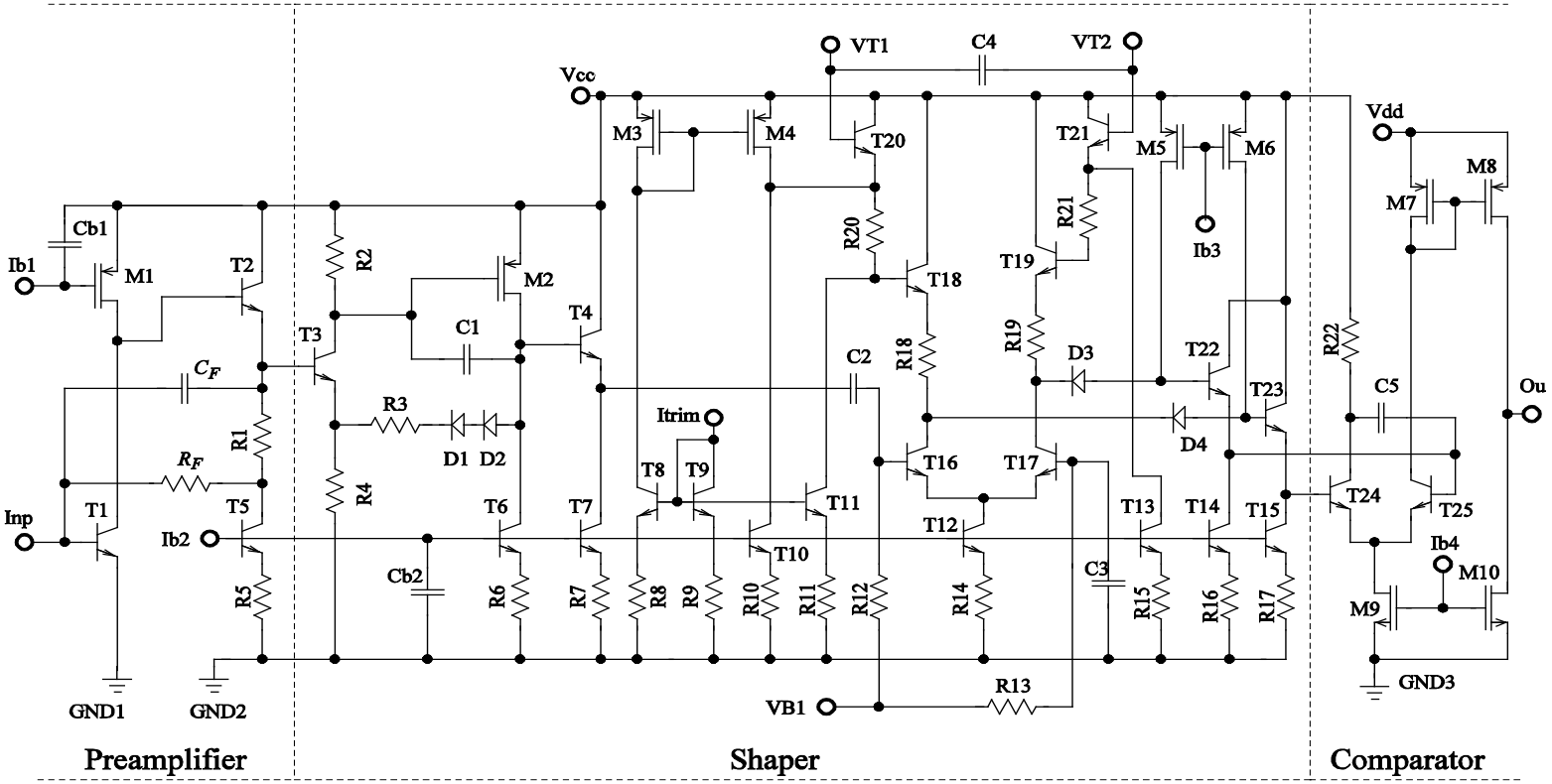
For AC coupled detectors:

- Resistive feedback, (a)
- Active feedback, (b)
- Active feedback with non-linearity compensation, (d)

For DC coupled detectors (leakage compensation):

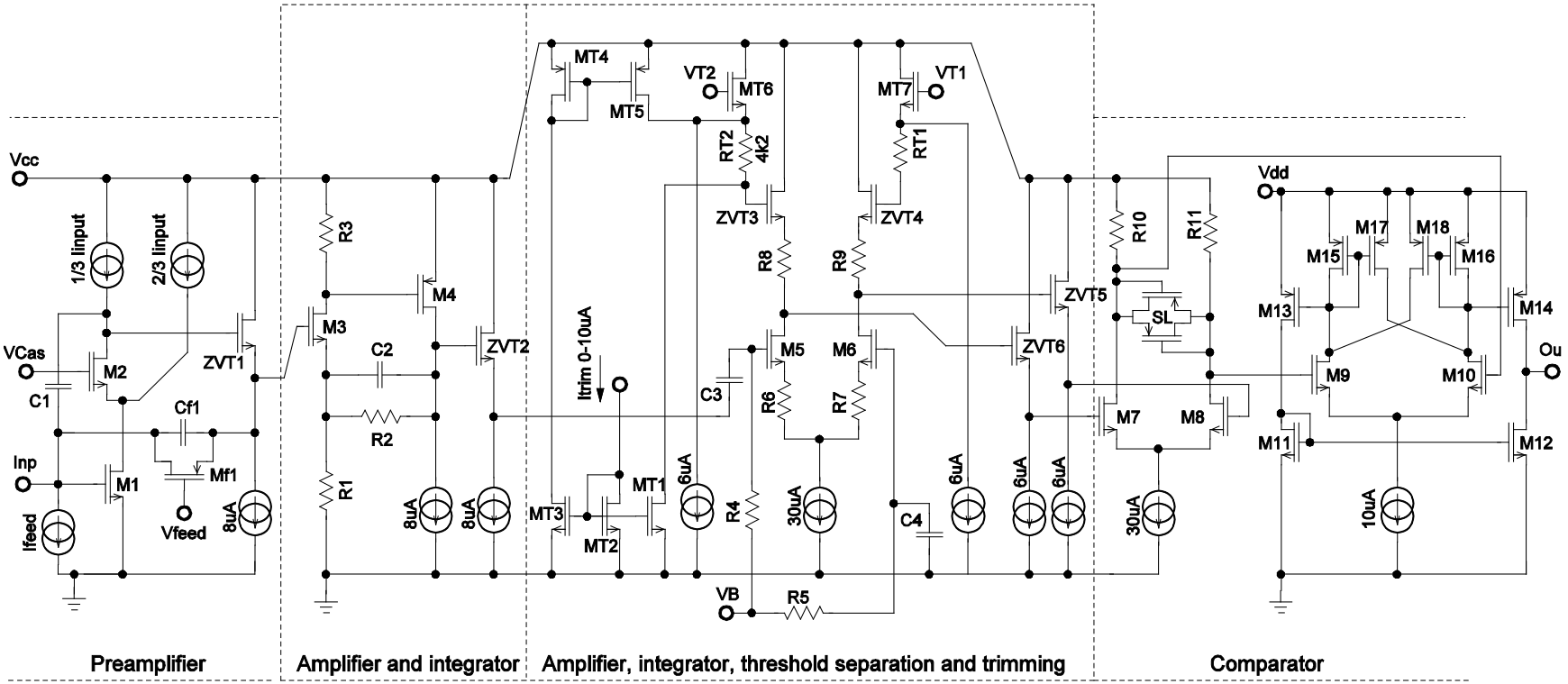
- With some limits type (a) and (d)
- Krummenacher feedback (c)

Front end channel in BiCMOS technology (present ATLAS SCT)



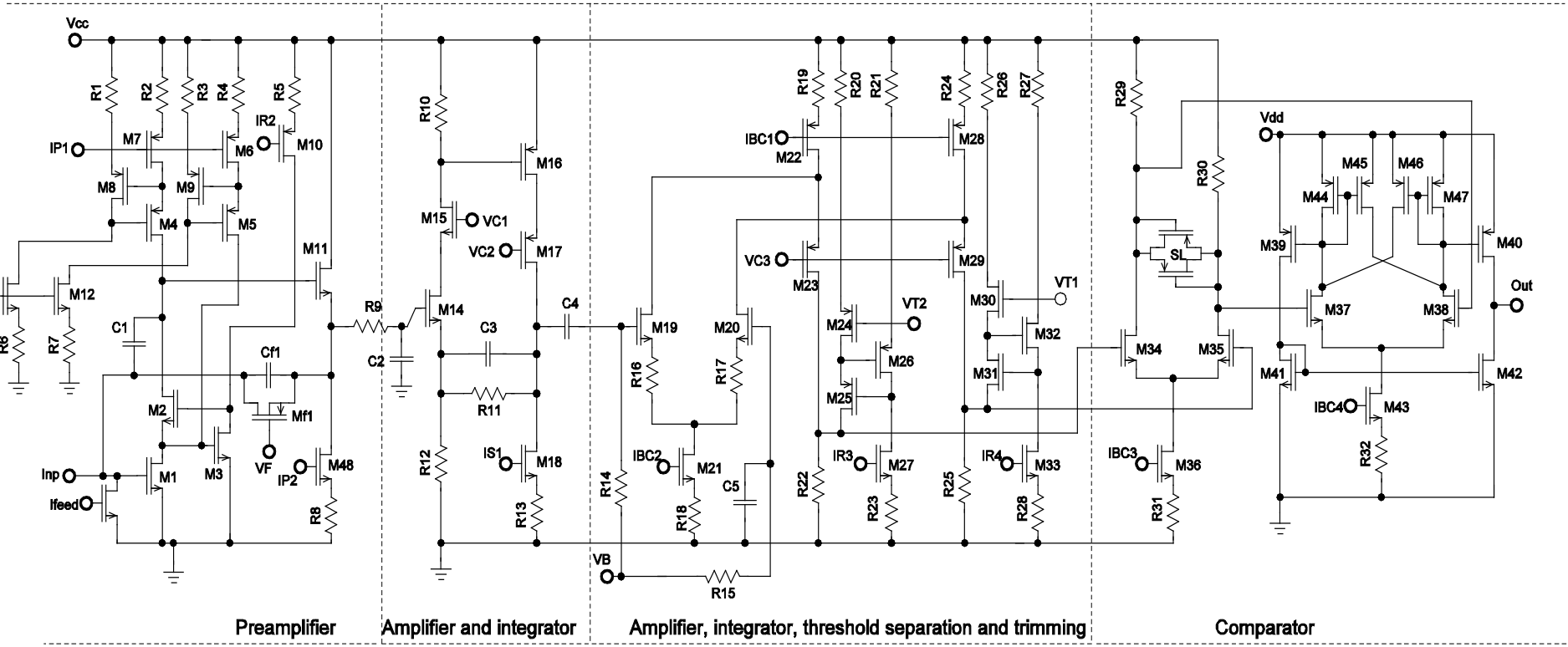
- Optimized for detector capacitances of about 20pF
- Input stage: 1GHz GBP, 65dB open loop gain
- Peaking time 25ns, power consumption 1.7mW/channel (3.5V supply)

Front end channel in CMOS 250nm technology (ATLAS, TOTEM experiment, CT head)



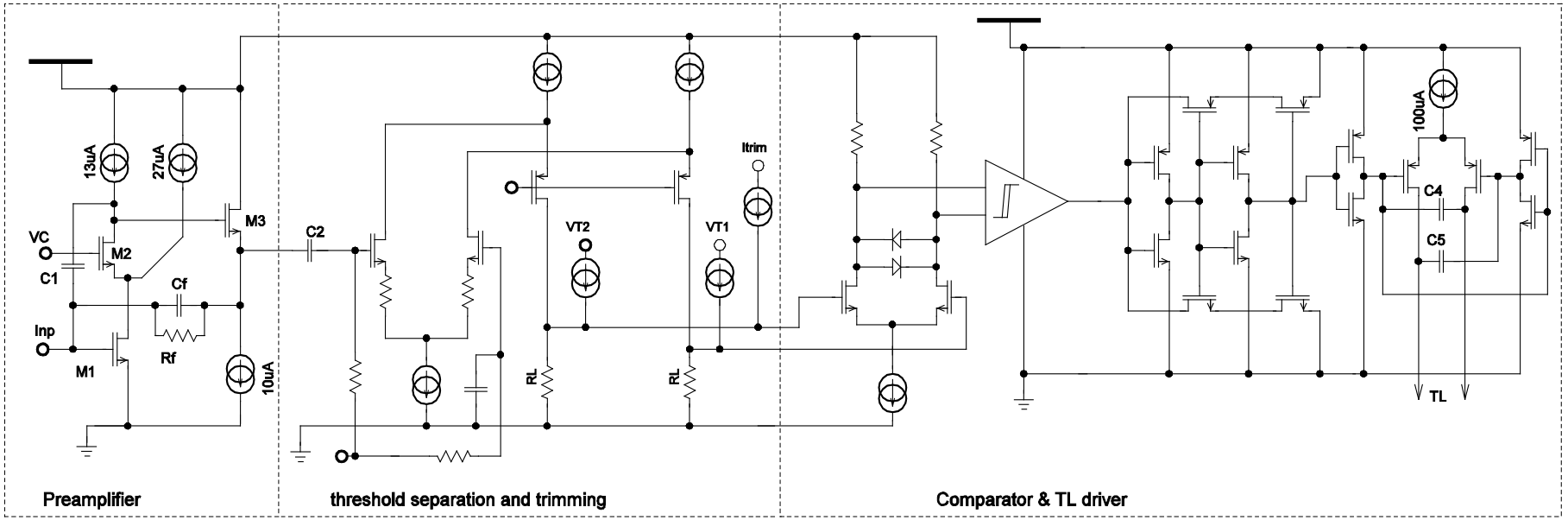
- Various versions optimized for detector capacitances from 5 to 30pF
- Input stage: 0.6-1GHz GBP, 85dB open loop gain
- Peaking time 22ns, power consumption 0.7-1.5mW/channel (2.5V supply)

Front end channel in 130nm CMOS technology (SCT short strips)



- Optimized for detector capacitances from 5 to 10pF
- Input stage: 2GHz GBP, 80dB open loop gain
- Peaking time 22ns, power consumption 0.2-0.3mW/channel (1.2V supply)

Fast (5ns) front end for pixel (130nm CMOS)



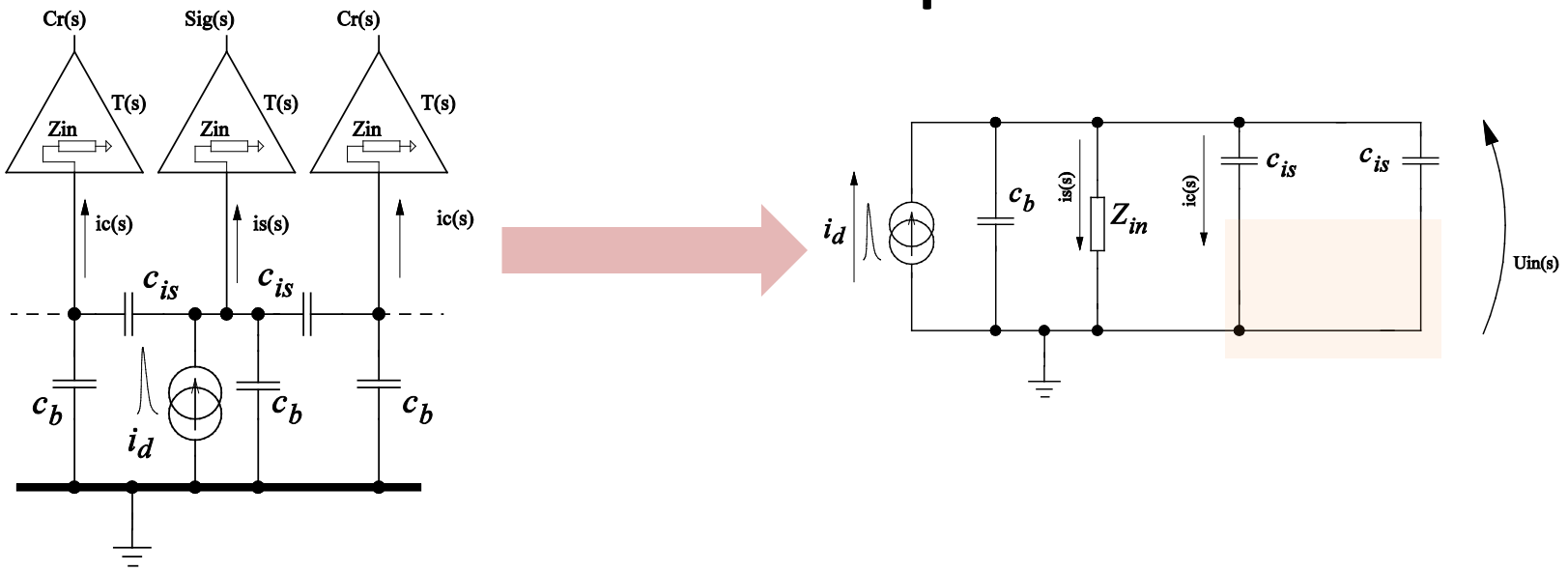
- Optimized for detector capacitances around 250fF
- Input stage: 2GHz GBP, 47dB open loop gain
- Peaking time 5.5ns, power consumption 0.12mW/channel (1.2V supply)

Summary

- Power consumption is a key issue in HEP applications
- Front end electronics for semiconductor detectors → results of trade off between noise, power and speed requirements
- Parameters of input stage define overall performance of front end in terms of noise, charge collection efficiency, crosstalk signals, phase margin and PSRR
- Technology scaling: new opportunities but there are also some new problems...

supplement

Crosstalk calculation; currents at front end inputs



Simplified model; assumption that input of the preamplifier is loaded with c_b and two c_{is} capacitances (neglecting input impedances of the neighbors). Using Kirchhoff law one can write:

$$i_d = u_{in} \cdot \left(s \cdot (c_b + 2 \cdot c_{is}) + \frac{1}{Z_{in}} \right)$$

i_d (s) =1 (delta Dirac)

$$u_{in} = \frac{Z_{in}}{1 + s \cdot (c_b + 2 \cdot c_{is}) \cdot Z_{in}}$$

Current flowing into readout channel

$$i_s = u_{in} \cdot \frac{1}{Z_{in}}$$

Crosstalk signal (we assume that current flows into Z_{in} of neighbor through c_{is})

$$i_c = u_{in} \cdot \frac{1}{Z_{in} + \frac{1}{s \cdot c_{is}}}$$

Crosstalk calculation; example of response with CR-RC^2 filter

For example calculation we will consider CR-RC^2 type of the shaper. The transfer function in operator domain is following;

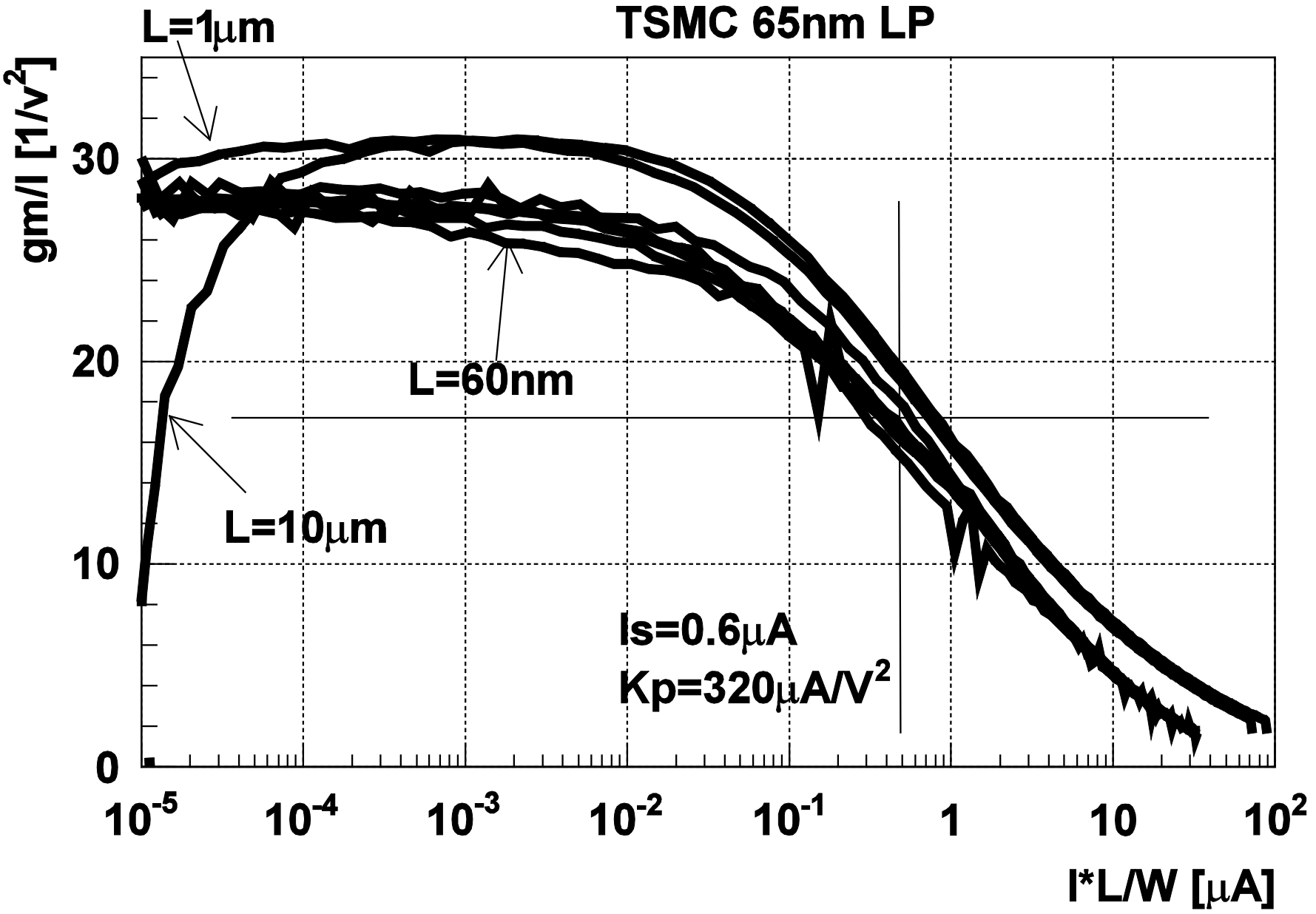
$$T_{FE} = \frac{\tau_f}{(1 + s \cdot \tau_f)^3}$$

The response of Front End to delta Dirac function in time domain will be:

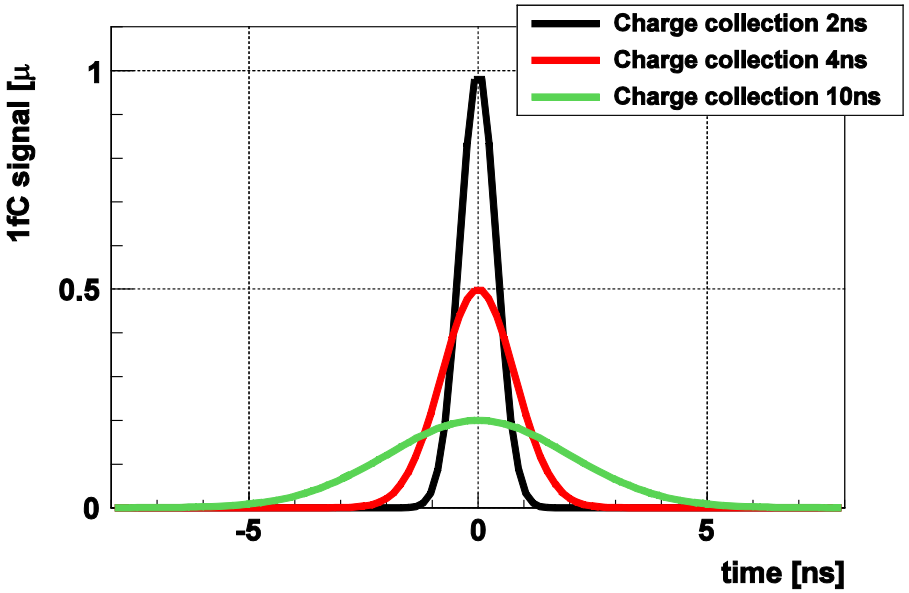
$$L^{-1}\left(T_{FE} \cdot i_s\right)$$

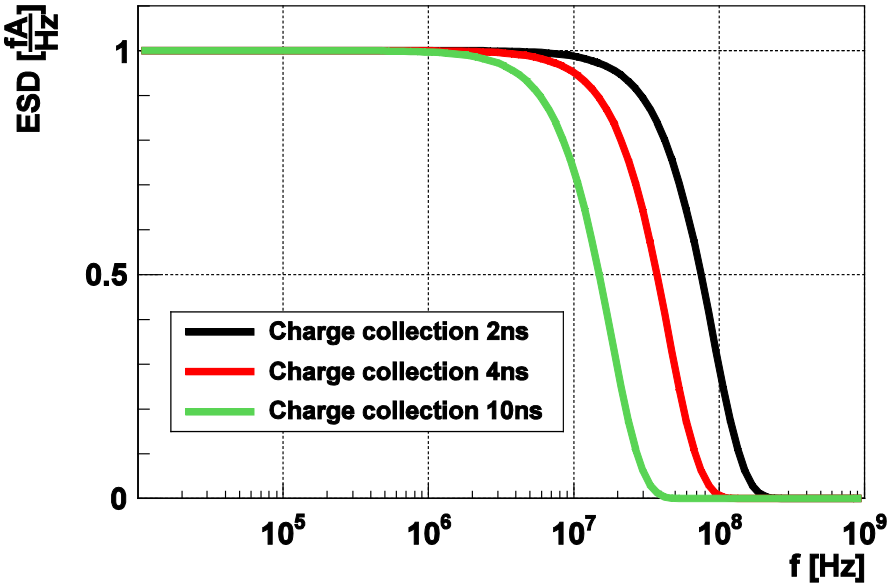
The crosstalk of first neighbor in time domain will be:

$$L^{-1}\left(T_{FE} \cdot i_c\right)$$

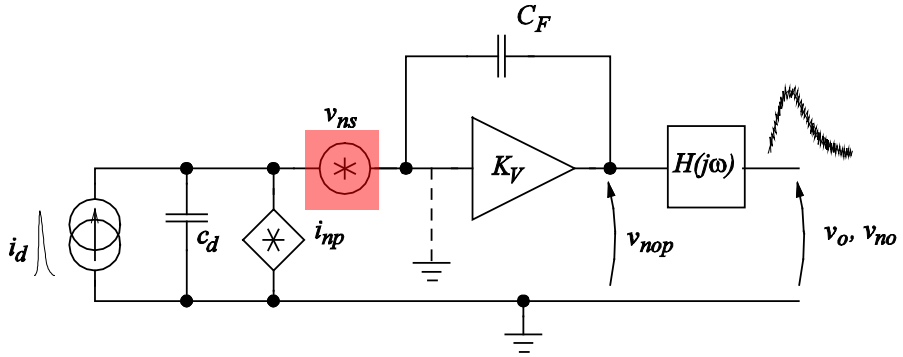

TSMC 65nm LP
L=1μm
L=60nm
L=10μm
Is=0.6μA
Kp=320μA/V2
gm/I [1/v2]
I*L/W [μA]
0
10
20
30
10-5
10-4
10-3
10-2
10-1
1
10
102

Frequency spectrum of the detector signal (Energy Spectrum Density -ESD)





Minimization of serial noise – driving of g_m



$$\frac{\overline{v_{ns}^{\,2}}}{\Delta f} = \frac{4 \cdot k \cdot T \cdot n \cdot \gamma}{g_m}$$

$$ENC^2[C] = F_V^2 \cdot \frac{\overline{v_{ns}^2}}{\Delta f} \cdot c_d^2 \Big/ t_{peak} \quad + \quad F_i^2 \cdot \frac{\overline{i_{np}^2}}{\Delta f} \cdot t_{peak}$$