Calculation of the ENC for Charge Sensitive Amplifiers (CSA) built with CMOS devices

In well-designed input stage of the CSA the series noise contribution comes from the input device. Assuming sufficient pulse gain of the preamplifier and careful design of the input stage it is a reasonable approximation, allowing for great simplification of the analytical analysis. Another noise sources taken into account during the presented analysis will be parallel noise related to the feedback circuit (resistor or active devices) as well as detector leakage current.

In order to describe accurately the noise performance of the MOS transistor for a wide range of the bias currents and transistor dimensions, one must calculate precisely the transconductance and intrinsic gate capacitances for each current density. In our work we have used an analytical EKV model [1], which provides continuity between weak, moderate and strong inversion. Since the presented analysis is focused on the noise performance of MOS devices we simplify the general model assuming that the transistors work in saturation, between the weak and moderate inversion.

I.A. Modeling of the transconductance and intrinsic gate capacitance

The classical formulae describing the transconductance in the EKV model are given by (1) to (3). The specific current I_S, used for the normalization is described as:

$$I_S = 2\ n\ \beta\ U_T^2 \quad \text{where} \quad \beta = K_P\ \frac{W}{L}\ , \quad U_T = \frac{k\ T}{q} \tag{1}$$

The transconductance of the MOS transistor is normalized to the maximum value, which can be reached in the weak inversion. The function used for interpolation of the transconductance between strong and weak inversion for a given drain current I_D is described by:

$$G(I_f) = \frac{1}{\sqrt{I_f + \frac{1}{2}\ \sqrt{I_f} + 1}} \qquad \text{where} \quad I_f = \frac{I_D}{I_S} \tag{2}$$

Finally the transconductance of a MOS transistor biased in weak and moderate inversion is given by:

$$g_m = G(I_f)\ \frac{I_D}{n\ U_T} \tag{3}$$

Fig. 1 shows a comparison between the transconductance simulated with the EKV model and measured for an NMOS transistor of dimensions 2000µm/0.5µm, covering the weak and moderate inversion regions of operation.

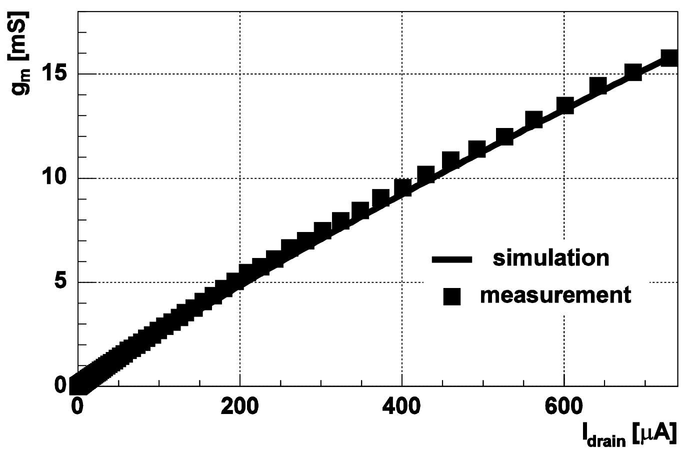

Figure 1 **Comparison between measured and calculated transconductances of an NMOS transistor of dimensions 2000µm/0.5µm for a wide range of drain current (IBM 250nm process).**

For the deep submicron processes (65nm and below) it is worth to take into account the velocity saturation of the carriers in the transistor channel. This is especially important for the inversion coefficient above 1 (moderate to strong inversion region). The extra technological parameter to be included in the calculation is the critical electric field (EC). The length of the channel which is in velocity saturation L_{SAT} and the fraction of the channel in full velocity saturation λ_C are described as following:

$$L_{SAT}=\frac{2\ U_T}{E_C} \qquad \lambda_C=\frac{L_{SAT}}{L} \tag{3a}$$

The transconductance of the MOS transistor is normalized to the maximum value, which can be reached in the weak inversion. The function used for interpolation of the transconductance between strong and weak inversion for a given drain current I_D including velocity saturation effect is described by [2]:

$$G_{VS}(I_f)=\frac{\sqrt{(\lambda_C\ I_f\ +\ 1)^2\ +\ 4\ I_f}\ -1}{I_f\ (\lambda_C\ (\lambda_C\ I_f\ +\ 1)\ +2)} \qquad \text{where} \qquad I_f=\frac{I_D}{I_S} \tag{3b}$$

Finally the transconductance of a MOS transistor biased in any inversion region taking into account the velocity saturation effect is given by:

$$g_m=G_{VS}(I_f)\ \frac{I_D}{n\ U_T} \tag{3c}$$

Another transistor parameter which needs to be calculated is the gate capacitance. It is a sum of the intrinsic gate capacitance and the gate-to-source and gate-to-drain overlap capacitances. For a MOS transistor working in saturation the intrinsic gate capacitance has two components described by the following formulae:

- gate-to-source capacitance:

$$C_{GS}=C_{OX}\left(\frac{1}{I_f\ G(I_f)}+\frac{3}{2}\right)^{-1} \qquad \text{where} \quad C_{OX}=W\,L\ \frac{\varepsilon_{OX}}{t_{OX}} \tag{4}$$

- gate-to-bulk capacitance:

$$C_{GB}=C_{OX}\ \frac{n-1}{n}\left(1-\frac{I_f\ G(I_f)}{1+\frac{3}{2}\ I_f\ G(I_f)}\right) \tag{5}$$

I.B. *Modeling of noise*

For calculation of the thermal noise we use the model proposed by van der Ziel [3], but slightly modified for weak and moderate inversion regions [1]. For relatively large MOS transistors, we take into account the gate induced current noise (GIC), since its spectral density is proportional to the gate capacitance C_{OX} .

Taking into account both transconductances, g_m and g_{mb}, contributing to the channel thermal noise, the spectral density of the thermal noise, i_{nd}, in the MOS transistor can be described by the following equation [1]:

$$\overline{i_{nd}^2} = 4\ k\ T\ G_{Nth}\ \Delta f \quad \text{where} \quad G_{Nth} = \gamma\ (g_{mb} + g_m) = \gamma\ n\ g_m \tag{6}$$

The bias dependent parameter γ takes values from 1/2 to 2/3 for the ideal transistor operating in the weak and the strong inversion respectively. The model works well for long channel devices. The excess noise observed in short channel devices can be modeled using numerical methods [4]. In a more practical approach one introduces an excess noise factor G. It can be incorporated together with an interpolating function $F_n(I_f)$ determining the γ factor for a given region of operation:

$$\gamma = F_n(I_f) \cdot G \quad \text{where} \quad F_n(I_f) = \frac{1}{1 + I_f} \left(\frac{1}{2} + \frac{2}{3}\ I_f \right) \tag{7}$$

The spectral density of the high frequency GIC noise was originally analyzed by van der Ziel for an ideal MOS transistor working in saturation and strong inversion [3]. According to [4], the high frequency GIC excess noise rises together with the excess thermal noise. This is expected since the origin of the GIC noise is the coupling of fluctuations of the current thermal noise from the transistor channel. Consequently the gate induced current noise for a non-ideal device, independently of the region of operation can be estimated as follows [3]:

$$\overline{i_{ng}^2} = 8\,\gamma\,k\,T\,g_{gs}\,\Delta f \quad \text{where} \quad g_{gs} = \frac{4}{45}\frac{\omega^2\,C_{OX}^2}{n\,g_m} \tag{8}$$

For complete evaluation of thermal noise in the MOS transistor one has to take into account the correlation between channel thermal noise i_{nd} and gate induced noise i_{ng}. For the correlation coefficient equal to $j\sqrt{5/32}$ [2] one obtains the correlation term as:

$$\overline{i_{ng}\ i_{nd}^*} = \frac{\gamma}{6}\ j\,\omega\,C_{OX}\ 4\ k\,T\ \Delta f \tag{9}$$

The next source of noise taken into account in this analysis is the flicker noise. In the commonly used model of the flicker noise, the current noise generator is placed in-between the drain and source of the MOS transistor. The power spectral density is given as:

$$\overline{i_{nf}^2} = \frac{K_a}{f}\,\frac{g_m^2}{C_{OXU}^2\,W\,L}\,\Delta f \qquad \text{where} \quad C_{OXU} = \frac{\varepsilon_{OX}}{t_{OX}} \tag{10}$$

The equivalent schematic of the transimpedance preamplifier including all discussed noise sources related to the input transistor and the feedback circuit is shown in Fig. 2.

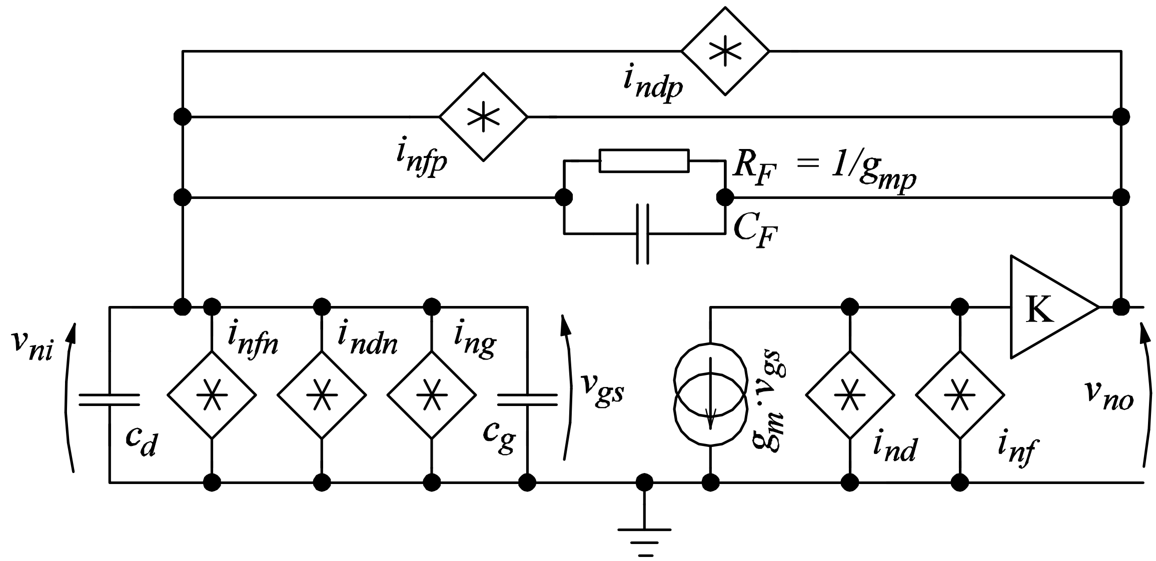

Figure 2 **Equivalent schematic of the MOS transimpedance preamplifier with active feedback including all noise sources related to the input transistor and feedback circuit.**

I.C. Calculation of the preamplifier output noise

Assuming that the circuit is linear one can identify the contributions to the output noise from each noise source described by (6), (8) and (10), separately. Although for the elementary noise sources the propagation of the noise fluctuation to the preamplifier output may be calculated directly in the frequency domain, the calculation of the correlation term between thermal and GIC noise is more complex. For clarity let us consider only two noise sources i_{ng} and i_{nd}.

Assuming sufficiently wide bandwidth and high gain of the preamplifier stage and using elementary network theory one finds the output noise in the time domain as:

$$v_{no}(t)=\frac{i_{nd}(t)}{g_m} Z_F\, Y_T + i_{ng}(t)\, Z_F \tag{11}$$

where:

$$Y_T = Y_F + Y_g + Y_d, \quad Z_F = \frac{1}{Y_F} = \frac{R_F}{1+j\omega\tau_f}, \quad \tau_f = R_F\, C_F \tag{12}$$
$$Y_d = j\,\omega\, c_d, \quad Y_g = j\,\omega\, c_g$$

Expanding the noise sources for Fourier series:

$$i_{nd}(t)=\sum_{n=-\infty}^{\infty} a_n \exp(j\omega t) \tag{13}$$

$$i_{ng}(t)=\sum_{n=-\infty}^{\infty} b_n \exp(j\omega t) \tag{14}$$

$$v_{no}(t)=\sum_{n=-\infty}^{\infty} d_n \exp(j\omega t) \tag{15}$$

and inserting them into (11) one finds the following relation between n-terms of Fourier series:

$$d_n = a_n \frac{Z_F}{g_m} Y_T + b_n Z_F \tag{16}$$

Consequently, the spectral density of the output noise is given as:

$$\frac{\overline{v_{no}^2}}{\Delta f}=\overline{d_n\, d_n^*}=\overline{\left(a_n\frac{Z_F}{g_m}\,Y_T+b_n\,Z_F\right)\left(a_n^*\frac{Z_F^*}{g_m}\,Y_T^*+b_n^*\,Z_F^*\right)} \tag{17}$$

After some algebra one obtains:

$$\frac{\overline{v_{no}^2}}{\Delta f}=\overline{a_n\, a_n^*}\,\frac{|Z_F|^2}{g_m^2}|Y_T|^2+\overline{b_n\, b_n^*}\,|Z_F|^2+2\,\mathrm{Im}\left[\overline{b_n\, a_n^*}\right]\frac{|Z_F|^2}{g_m}\,|Y_T| \tag{18}$$

Then, using (6), (8) and (9) one obtains the following expression for the spectral density of the output noise:

$$\frac{\overline{v_{no}^2}}{\Delta f}=\frac{\overline{v_{no\_id}^2}}{\Delta f}+\frac{\overline{v_{no\_GIC}^2}}{\Delta f}+\frac{\overline{v_{no\_corr}^2}}{\Delta f} \tag{19}$$

where:

$$\frac{\overline{v_{no\_id}^2}}{\Delta f}=\frac{4\,k\,T\,\gamma\,n}{g_m}\left(\omega^2\left(c_d+c_g+C_F\right)^2+\frac{1}{R_F^2}\right)\frac{R_F^2}{1+\tau_f^2\,\omega^2} \tag{20}$$

$$\frac{\overline{v_{no\_GIC}^2}}{\Delta f}=\frac{32}{45}k\,T\,\gamma\frac{\omega^2\,C_{OX}^2}{n\,g_m}\,\frac{R_F^2}{1+\tau_f^2\,\omega^2} \tag{21}$$

$$\frac{\overline{v_{no\_corr}^2}}{\Delta f}=\frac{8}{6}\frac{\gamma\,k\,T}{g_m}\omega^2\,C_{OX}\left(c_d+c_g+C_F\right)\frac{R_F^2}{1+\tau_f^2\omega^2} \tag{22}$$

Keeping in mind that c_g is much larger than C_F one can simplify (20) for the frequencies within the bandwidth of the shaper stage to:

$$\frac{\overline{v_{no\_id}^2}}{\Delta f}=\frac{4\,k\,T\,\gamma\,n}{g_m}\,\omega^2\left(c_d+c_g+C_F\right)^2\,\frac{R_F^2}{1+\tau_f^2\,\omega^2} \tag{23}$$

In a similar way one can find the contribution of the flicker noise to the preamplifier output noise as:

$$\frac{\overline{v_{no\_f}^2}}{\Delta f}=\frac{K_a}{f\,C_{OXU}^2\,W\,L}\omega^2\left(c_d+c_g+C_F\right)^2\,\frac{R_F^2}{1+\tau_f^2\,\omega^2} \tag{24}$$

I.D. Noise optimization of the input transistor

The rms noise at the output of ideal CR-(RC)^m shaper (since we consider the transimpedance preamplifier, the differentiation of the signal is provided by the feedback time constant and the shaper stage consist only of m integration stages), σ_{nfo}, can be calculated as:

$$\sigma_{nfo}=\left(\int_0^\infty\frac{\overline{v_{no}^2}}{\Delta f}\;\frac{1}{\left(1+\tau_f^2\;\omega^2\right)^m}\;\partial f\right)^{\frac{1}{2}} \tag{25}$$

where v_{no} represents all partial contributions of thermal noise, GIC noise, correlation term and flicker noise sources related to the input transistor (equations (21), (22), (23) and (24)). Finally the ENC is calculated as following:

$$ENC\,[e^-] = \frac{\sigma_{nfo}}{q\;Gain} \quad \text{where} \quad Gain = \frac{e^{-m}\,m^m}{C_F\,\Gamma(m+1)} \tag{26}$$

where Γ stands for gamma function.

Each term of (25) corresponding to different noise source can be integrated separately to find the partial contribution to equivalent noise charge. The contributions of the thermal, GIC and flicker noise as well as correlation term related to the input transistor are as follows:

$$ENC_{Id}[e-] = 2^{-\frac{1}{2}-m}\, e^m m^{1-m} \sqrt{\Gamma(2m-1)} \sqrt{\frac{4\,k\,T\,n\,\gamma}{g_m}}\; \frac{c_d + c_g + C_F}{\sqrt{t_{peak}}}\, \frac{1}{q} \tag{27}$$

$$ENC_{GIC}[e-] = \frac{2^{2-m}\, e^m m^{1-m}}{3\sqrt{5}} \sqrt{\Gamma(2m-1)} \sqrt{\frac{k\,T\,\gamma}{n\,g_m}}\; \frac{C_{OX}}{\sqrt{t_{peak}}}\, \frac{1}{q} \tag{28}$$

$$ENC_{If}[e-] = \frac{e^m m^{\frac{1}{2}-m}}{\sqrt{2}} \Gamma(m) \sqrt{\frac{K_a}{W\,L}}\; \frac{c_d + c_g + C_F}{C_{OXU}}\, \frac{1}{q} \tag{29}$$

$$ENC_{corr}[e-] = \frac{2^{\frac{1}{2}-m}\, e^m m^{1-m} \sqrt{\Gamma(2m-1)}}{\sqrt{3}} \sqrt{\frac{k\,T\,\gamma}{g_m}}\; \frac{\sqrt{C_{OX}\,(c_d + c_g + C_F)}}{\sqrt{t_{peak}}}\, \frac{1}{q} \tag{30}$$

The final ENC related to the input transistor can be obtained by quadratic summing of the partial contributions (27) to (30).

I.E. Modeling of the noise contribution of the active feedback loop

The equivalent schematic of the amplifier, including the noise sources associated with the feedback PMOS transistor and the NMOS current source (which determines the feedback current) is shown in Fig. 2. Both components contribute channel thermal noise (i_{ndp} and i_{ndn}) as well as flicker noise (i_{nfn} and i_{nfp}). One may depict the noise spectra density related to the feedback circuit v_{no_feed} at the preamplifier output as:

$$\frac{\overline{v^2_{no\_feed}}}{\Delta f} = \frac{R_F^2}{1+\tau_f^2\,\omega^2}\left(\overline{i^2_{nfn}} + \overline{i^2_{nfp}} + \overline{i^2_{ndn}} + \overline{i^2_{ndp}}\right) \tag{31}$$

Assuming a CR-(RC)^m shaper circuit and computing the integrals for the flicker and thermal noise separately for NMOS and PMOS transistor, one obtains the expressions for the corresponding ENC contributions from each noise source. The ENC contribution from the thermal noise of each feedback transistor is given as:

$$ENC_{feed-th}[e-] = \frac{e^m}{2^m} m^{-\frac{1}{2}-m} \sqrt{\Gamma(2m+1)} \sqrt{k\,T\,n\;\gamma\;g_m\,t_{peak}}\, \frac{1}{q} \tag{32}$$

Note that the definite integrals of the components related to the flicker noise of the feedback devices do not converge for frequencies decreasing toward zero. The problem is resolved by taking into account additional bandwidth limitation (AC coupling to the following stages or finite measurement time). Therefore to get an output rms noise we will integrate the noise spectra from FLL (frequency lower limit) and not 0. The result consists of incomplete beta function which is not possible to compute in the root program. The root routines use computed beta function from the Mathematica for a given parameter sets (FLL, t_{peak} and m)

$$ENC_{feed-1/f}[e-] \approx \frac{e^m m^{-m}\Gamma(1+m)}{m\sqrt{2}} \sqrt{-(-1)^{-m}\; \mathrm{B}\!\left(-\frac{m^2}{4\,\pi^2\,FLL^2\,t^2_{peak}}, 1+m, -m\right) g_m\,t_{peak}}\; \sqrt{\frac{K_a}{W\,L}}\; \frac{1}{C_{OXU}}\, \frac{1}{q}$$

(33)

Figure 3 shows the ENC (left axis) and the equivalent feedback resistance (right axis) as a function of the feedback current. The same plot shows for comparison the noise of an equivalent passive resistor.

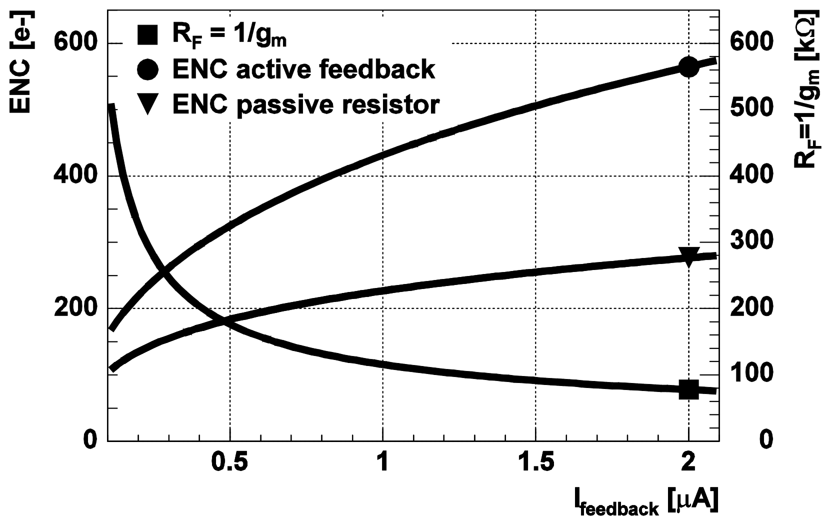

Figure 3 **Comparison of the ENC generated by an active feedback and by a passive resistor of the same equivalent resistance for the peaking time of 22 ns and the 3rd order CR-RC filter. Left axis shows the ENC and right axis shows the equivalent feedback resistance. IBM 250nm technology.**

The current required to obtain the feedback resistance in the range of 120 kΩ is around 0.8 μA. For this current the parallel noise due to the AFP circuit is about 400 e^- ENC, whereas the noise of a passive resistor in the feedback would be about 200 e^- ENC.

I.F. Passive feedback resistor and leakage current

In case of use a passive resistor in the feedback the current noise associated with this resistor is given by

$$\frac{\overline{i_{RF}^2}}{\Delta f} = \frac{4kT}{R_F} \tag{34}$$

The output noise related to the feedback resistor is the parallel noise source and can be calculated as following:

$$v_{no\_RF}(t) = i_{RF}(t) Z_F \tag{35}$$

The equivalent noise charge coming from the passive feedback resistor is:

$$ENC_{RF} = \frac{e^m m^{-m}}{2} \sqrt{2^{1-2m}\Gamma(2m)} \sqrt{\frac{4kT}{R_F}} \sqrt{t_{peak}} \frac{1}{q} \tag{36}$$

The ENC related to the detector leakage can be calculated as any other parallel noise source:

$$ENC_{leak} = \frac{e^m m^{-m}}{2} \sqrt{2^{1-2m}\Gamma(2m)} \sqrt{2qI_{leak}} \sqrt{t_{peak}} \frac{1}{q} \tag{37}$$

II. REFERENCES

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[4] Jung-Suk Goo et al., “An Accurate and Efficient High Frequency Noise Simulation Technique for Deep Submicron MOSFETs”, IEEE Transactions on Electron Devices, vol. 47, no. 12, December 2000, 2410-19.